Photonic Integrated Devices and Systems (PIDS): Technology for Next Generation Networks

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Malaviya National Institute of Technology Jaipur

- Established in 1961
- Constitutes of 13 Departments and 7 Centres of Excellence running 8 UG programs, 26 PG and doctoral programs.
- More than 6000 students on campus.

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Collaborative Research Project Partners

Keio University, Japan (2014-2016)

University of Vienna (2015-2017)


Cairo University Giza, Egypt (2016-2018)
Other Active Research Partners
Photonic Integrated Devices and Systems (PIDS)

Technology for Next Generation Networks

I extend my sincere thanks and pay regard to all contributors, whose texts/statements and pictures are referred in this presentation. The presentation is made for its exclusive use in academic purposes only.
Milestones of Optical Networking Technologies

- Discovery of Laser

- Mid-60s: Guided wave optics demonstrated

- Production of low-loss fibers
  - Made long-distance optical transmission possible!

- Invention of semiconductor laser diode
  - Made optical transceivers highly refined!

- Use of fiber in telephony: SONET
Milestones of Optical Networking Technologies

- Mid-80s: LANs/MANs: broadcast-and-select architectures

- 1988: First transatlantic optical fiber laid

- Late-80s: EDFA (optical amplifier) developed
  - Greatly alleviated distance limitations!

- Mid/late-90s: DWDM systems explode

- Late-90s: Intelligent Optical networks

- 2000: ……….. “O – O – O processing”

- 2005: ……….. PICs applications & smart networks
Pressure on Telecom networks:

(Power hungry Internet applications)

Alternate Solutions: PICs

Benefits:

- High BW/Speed
- Secure
- Immune to Noise/EMI
- Cost effective
Why Photonic Interconnects?

- Electrons are charged particles. They are fermions. Electronic crosstalk is inherent.
- Photons are bosons. They don’t interact. Crosstalk is minimal. 50 Tbps on a waveguide is possible.
- For short lengths, power to drive an electrical connection is proportional to its length.
- Power to drive an optical connection is the same for 1 micron to 100 km.

[Diagram showing power requirements for optical vs electrical interconnects]

Minimum on-chip power dissipation at 1Gbps
(Ref: R. A. Nordin et al.)
Popularity for PICs??

- Robust/Compact/Flexible:
- Energy efficient
- Reliability/Satisfactory performance.

Integrated Photonics:
- Planar Lightwave Circuits
- Integrated optoelectronic devices
- Wafer-scale technology on substrates (chips)
- Technology limitations
Integrated Electronics v/s Integrated Photonics

- Transistor: 1947, EIC = 1954; OICs: 1969
- Exponential growth of EIC Industry
- Operation & fabrication difference
- PICs: equivalent to EICs

Growth rate of PICs compared with CMOS ICs (Moore’s Law) [8]. Predicted by Rod Tucker.
Progress (PICs)

- Cause for Initial slow progress
- Major breakthrough: Invention of semiconductor LEDs/LDs and SOA
- Missing factor: Lack of standard fabrication and packaging technology
- Functional devices (PICs application):
  - (amplification, attenuation, multiplexing, demultiplexing, modulation, coupling, switching, lasing, detection etc.)
- First commercial application: (2005), Infinera DTN
  - (DWDM platform based on a 100G PIC operating with 10 channels of Intensity Modulation of 10 Gb/s with Direct Detection (IM-DD).)
Photonic Integrated Circuits - Technologies

- Silicon Photonics
- Silica-on-Silicon - Silica glass (fused Silica)
- III-V Integration Platforms
- Polymer Integration Platforms

**PIC Development Approaches:** Si v/s III-V Photonics

- Silicon: Availability/Versatility/Low cost/Compatible.

- III-V semiconductors:
  a) high-power and high-frequency applications
  b) high light emission efficiency (laser applications).
Silicon Photonics

- Track record of success
- Compatibility with EIC fabrication technology
- Performance, yield, robust, reproducible.
- Production of PICs in high volumes/economically
- Unique possibility of integrating electronic/optical functions on the same chip
- Transparent for telecom windows
- High packing density
Applications

- Ability to reuse the huge technology base and supply chain from electronics industry
- Photonic components (modulators, detectors, sources) fully compatible with CMOS technology.

Challenges:

- Indirect band gap (Si): Laser source integration??, Poor absorber at 1550nm (How to build PD??).
- Attenuation, inter-channel interference and polarization must to avoid/control for long distance telecom applications.
Towards Si laser ....

Approaches:

- **Hybrid silicon PIC technology**
  bonding of functional III-V active components onto silicon-on-insulator substrates

- **Bonding of III-V epitaxial layers**
  wafer or die bonding of III-V films on Si and processing thereof

- **Hetero-epitaxial growth of III-V on Si**
  selectively grow III-V crystals on Si substrate

- **Selective growth of Germanium on Si**
  growth of Ge layers on silicon oxide trenches
Advantages:

- Solutions for: Lasers, Optical amplifiers, Modulators, Detectors
- Monolithic integration of passive/active components within fully functional chips
- Ultra-high speed EO characteristics
- High reliability

Disadvantages:

- Extensive integration approach
- Higher prop. losses
- Limitations of mass production
- Low index contrast (Δn/n)
III-V Semiconductor Technology: Applications

III-V monolithic integration of complex devices for...

- Telecom (1)-(3)
- Datacom (5),(7)
- Sensing (4),(6)
- Bio-Medical (8)

Hybrid integration on Si-based platforms

- WDM receiver for FTTH (user Genesis, fab HHI)
- Filtered Feedback MW laser (user ASTRON, fab Oclaro)
- hybrid TDM-WDM transmitters (user Genesis, fab Oclaro)
- FBG-readout (user Fibresensing, fab HHI)
- 4x4 space and λ-selective switch (user TU/e, fab COBRA)
- Pulse serialiser for KM3NeT neutrino detector (user NIKHEF, fab Oclaro)
- Pulse regenerator (user U Pisa, fab COBRA)
- Pulse shaper for bio-imaging (user LMU Munich, fab Oclaro)

ICT-GALACTICO
ICT-BOOM
ICT-RAMPLAS

GaAs - InP-based hybrid integration on SOI platform:
InP SOAs bonded on Si platform
GaInNAs(Sb) SOAs flip-chip bonded on SOI
Scaling of the data capacity/chip for InP-based transmitter chips utilized in optical telecom networks.

- The data capacity per chip has doubled on average every 2.2 years and is targeted to continue at this rate with the 500-Gb/s devices currently under development.
- The 100-Gb/s PICs are based on OOK, whereas the 500-Gb/s utilize PM-QPSK.

Courtesy: Fred A. Kish et al., IEEE JSTQE 2011
InP v/s Si Integrated Photonics

Why is the slope higher?
- Better process control
- More advanced process technology
- More uniform materials

Si vs In$_x$Ga$_{1-x}$As$_y$P$_{1-y}$ for core
SiO$_2$ vs In$_x$Ga$_{1-x}$As$_y$P$_{1-y}$ for cladding

Which will go higher? (Higher level of Integration)
Silicon because
- Wafer size is larger
- Process equipment can handle larger wafers
- Economic driver is integration on Silicon ICs (market is >100x larger)
- PCB/Backplane/Interrack/Data Center/Teleco

Courtesy: Prof. John E. Bowers’ group, UCSB, California
Glass: Overview

Main technology implementations:

- silica-on-silicon
- laser inscription on glass
- TriPlex

How it works:

- Waveguiding in glass (SiO2)
- Introduce dopants to create index difference (small to medium): similar material & dopants used in optical fibers.
- SiO2 surrounded/encapsulated by high index Si3N4 cladding/box section
**Glass: Key characteristics**

**Advantages:**
- Low prop. losses
- Low polarization dependence
- Broad wavelength coverage
- Low-loss coupling to SMF
- Weak TO-effect
- Reliable material, tolerance to environmental

**Disadvantages:**
- Low density integration
- Limited active functionalities
- Not efficient for λ-tuning functions
- Costlier fabrication

**Applications:**
- Passive components *(commercial)*
  - WDM multiplexers, FTTH splitters, TO-switches
- Hybrid integration of complex devices: III-Vs, LiNbO$_3$, Polymers
Polymers: Overview

Main material systems:
- SU-8, PMMA, ZPU-12, etc.
- Blending polymer solutions to achieve precise control of material optical properties

Main types of polymer platforms:
- Passive
- Electro-optic
- Active
Polymers: Key characteristics

Strengths:

- Low prop. loss (<0.5 dB/cm)
- Low birefringence
- Precise and continuous engineering of material properties
- Unique properties (large TO, EO, non-linear)
- Easy ability to process.
- Ease of hybrid integration via butt coupling

Weaknesses:

- Low index contrast, bulky device Not suitable for high temperature process.
- Some materials raise reliability issues.
- No full suite of active functionalities available out of the lab
Polymer PICs: Applications

Hybrid Optical/Electrical datacom PCBs:

- Waveguide PCB integration
- Cards for optical backplane

40G and 100G communication applications:

- High speed MZMs
- Variable optical attenuator arrays
PICs: Competitive history

Electronic-photonic integrated chip (IBM 2012)

Features:
- Optical modulators and Ge PDs, 25 Gbps
- Capable of shuttling data around at Tbps.

Integrated wavelength multiplexed Silicon photonics chip (IBM 2015)

Features:
- Support electrical/optical circuits on the same chip package
- Used in a "datacenter interconnect" setup that could push 100Gbps over a range of up to 2 Kms (1.24 miles).
Knights Mill: Si photonics product by Intel developer forum
SFO (US), August 2016

Features:
- Si–ICs: Speed 100 Gbps over a distance of 2 Km.
- Target applications: connectivity for cloud and enterprise datacenters as well as Ethernet switch, router, and client-side telecom interfaces.
- MS-Azure datacenters

Knights Mill stages:

The Xeon Scalable Platform: Xeon Phi for parallel acceleration and AI training (Machine Learning)

The Xeon Phi roadmap:
45nm Knights Ferry (2010), 22nm Knights Corner (2012), 14nm Knights Landing (2016)

What Next: 10nm Knights Hill (KNH) by 2020 with the Argonne National Laboratory to build the Aurora supercomputer.
Cloud Xpress 2 with infinite capacity engine (ICE)

- 100 gigabit Ethernet (100GbE) data center interconnect (DCI) over multi-terabit optical links.

- Can delivers a 1.2 Tb/s super-channel in only one rack unit while enabling best in class fiber capacity with up to 27.6 Tb/s on a single fiber pair.
Recent trends

Plasmonics

Potential applications:
- Chip-scale communications: Interconnects
- Sensing: Biosensors, lab-on-a-chip

Photonic Crystals

Carbon-based materials

Graphene/Carbon nanotubes (CNT)
Targets (PICs):

- To get the lasers on-package using III-V semiconductors (IBM).
- Next step: Get the lasers, waveguides, photodiodes, and other optical gubbins right onto the processor die itself, alongside the copper wires and transistors (IBM).
- Deploying Si Photonics technology for switch-to-switch interconnectivity at 100 Gbps and then to scale to even higher bandwidth — up to 400 Gbps in the near future.
- Development of PICs with use of Plasmonics, PCs, etc.
- To tackle fabrication challenges to trade-off the power requirements, cost and the chip area coverage.
Due to increasing demand of telecommunication market, the development of PICs has already taken a pace which is comparable to Moore’s law for microelectronics devices.

Applications (non telecom uses):
sensors, medical diagnostics, metrology or switching will also benefit with this development these all-optical or electro-optic devices.

Avoid the economic hurdles:
The technology involves for such integrated devices should also be compatible with the complementary metal-oxide- semiconductor (CMOS) fabrication.

Limiting factors (in telecom networks appl.)
various performance parameters such as operating range, transmission losses, and polarization dependence.
Designs @MNIT Labs

All optical devices (for PIDS appl.):
Switches, Couplers, Splitters, Logic Gates & Circuits
All Optical switches/Copulers

2 × 2 switch block with switching states: the "bar" state; and the "cross" state

Performance parameters:
- Insertion loss,
- Extinction ratio,
- Polarization-dependent loss,
- Crosstalk,
- Switching time,
- Reliability,
- Energy usage,
- Scalability,
- Temperature resistance, etc.

Materials:
- Si, SOI, InP, InGaAsP, InGaAs, AlGaInAs, LiNbO$_3$, Ti: LiNbO$_3$

Application:
- Optical Cross-Connects (OXC)s
- Protection Switching.
- Optical Add/Drop Multiplexing.
- Optical Signal Monitoring.
Conventional Switch/Coupler Structures

MZI structure

Stability of Mach–Zehnder modulator with increasing waveguide power levels

Temporal stability of Mach–Zehnder modulator for a waveguide power level of 75 mW

Design Guidelines

Length of the interferometer arm.

Coupling area of the constituent 3 dB couplers.

Unequal Interferometer arm and shape optimization.

Effect of changes in electrode dimension

Electro-optic MZI switches – state transition through voltages to the electrodes

The control sensitivity, control voltage range, equivalence in switching performance in different states considered.
Power imbalance of first stage 3-dB coupler

The imbalance factor (non-uniformity) and the generated CT levels due to $Q_1$ and $Q_2$ are calculated as follows [5].

The CT levels at the end of interferometric arms, prior to 2$^{nd}$ 3-dB combiner.

$Q_1$ and $Q_2$ are power levels at the end of interferometric arms.
<table>
<thead>
<tr>
<th>Operating wavelength (µm)</th>
<th>Optimized Ti-strip thickness (µm)</th>
<th>Min. req. Switch volt. (V)</th>
<th>CT levels (-ve dB)</th>
<th>I.L. (dB)</th>
<th>E.L. (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bar state</td>
<td>Cross state</td>
<td>Bar state</td>
</tr>
<tr>
<td>Ti-indiffused z-cut LN based MZI switch with path delay (tapered) arm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.3</td>
<td>0.054</td>
<td>Not req.</td>
<td>22.56</td>
<td>41.73</td>
<td>0.23</td>
</tr>
<tr>
<td>1.55</td>
<td>0.0825</td>
<td>Not req.</td>
<td>21.22</td>
<td>39.66</td>
<td>0.49</td>
</tr>
<tr>
<td>Ti-indiffused z-cut LN based EO-MZI switch with buffer layer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.3</td>
<td>0.054</td>
<td>7.2</td>
<td>29.68</td>
<td>41.73</td>
<td>0.023</td>
</tr>
<tr>
<td>1.55</td>
<td>0.0825</td>
<td>8.25</td>
<td>32.99</td>
<td>39.66</td>
<td>0.008</td>
</tr>
<tr>
<td>Ti-indiffused z-cut LN based EO-MZI switch without buffer layer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.3</td>
<td>0.054</td>
<td>4.6</td>
<td>30.99</td>
<td>41.73</td>
<td>0.023</td>
</tr>
<tr>
<td>1.55</td>
<td>0.0825</td>
<td>5</td>
<td>23.89</td>
<td>39.66</td>
<td>0.024</td>
</tr>
<tr>
<td>Ti-indiffused x-cut LN based EO-MZI switch with buffer layer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.3</td>
<td>0.054</td>
<td>10.5</td>
<td>29.77</td>
<td>17.20</td>
<td>0.033</td>
</tr>
<tr>
<td>1.55</td>
<td>0.0825</td>
<td>12</td>
<td>30.88</td>
<td>15.62</td>
<td>0.011</td>
</tr>
<tr>
<td>Ti-indiffused x-cut LN based EO-MZI switch without buffer layer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.3</td>
<td>0.054</td>
<td>4.7</td>
<td>30.89</td>
<td>17.20</td>
<td>0.032</td>
</tr>
<tr>
<td>1.55</td>
<td>0.0825</td>
<td>5.5</td>
<td>22.34</td>
<td>15.62</td>
<td>0.032</td>
</tr>
</tbody>
</table>
Multimode Interference (MMI) based switches

Self imaging principle: Along the direction of propagation of the multimode waveguide, an input field profile is reproduced in single or multiple images at regular intervals.

Tunable MMI−switches

Size modulated MMI−switches

Image modulated MMI−switches
## Tuning strategies (Example)

<table>
<thead>
<tr>
<th>Operating wavelength</th>
<th>Cross state</th>
<th>Bar state</th>
<th>3-dB state</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1.3µm</strong></td>
<td>All regions have same refractive index (n = 1.791)</td>
<td>n(&gt;)n' (n = 1.791, n' = n - δn)</td>
<td>n(&gt;)n' (n = 1.791, n' = n - δn)</td>
</tr>
<tr>
<td><img src="image1" alt="Cross state diagram" /></td>
<td><img src="image2" alt="Bar state diagram" /></td>
<td><img src="image3" alt="3-dB state diagram" /></td>
<td></td>
</tr>
<tr>
<td><strong>1.55µm</strong></td>
<td>n(&gt;)n' (n = 1.791, n' = n - δn)</td>
<td>n(&gt;)n' (n = 1.791, n' = n - δn)</td>
<td>n(&gt;)n' (n = 1.791, n' = - δn)</td>
</tr>
<tr>
<td><img src="image4" alt="Cross state diagram" /></td>
<td><img src="image5" alt="Bar state diagram" /></td>
<td><img src="image6" alt="3-dB state diagram" /></td>
<td></td>
</tr>
</tbody>
</table>
Inclusion of rearrangeable coupling regions for reducing PDL:

Region 7 and Region 8, each of 4µm wide, along with a little difference in their length, which are 16.36 µm and 16.48 µm respectively. However both regions can be made of same length, but in that case, observed PDLs are at higher levels (≥ 1dB).

Figure: Switch layout (structure–6).

Dimensions for extra IM regions

<table>
<thead>
<tr>
<th>Region</th>
<th>Width (W in µm)</th>
<th>Length (L in µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Region 4</td>
<td>4</td>
<td>54.2</td>
</tr>
<tr>
<td>Region 7</td>
<td>4</td>
<td>16.36</td>
</tr>
<tr>
<td>Region 8</td>
<td>4</td>
<td>16.48</td>
</tr>
</tbody>
</table>

State achieved

<table>
<thead>
<tr>
<th>Mode selected</th>
<th>Bar</th>
<th>Cross</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TE</td>
<td>TM</td>
</tr>
<tr>
<td>Wavelength(µm )</td>
<td>1.55</td>
<td>1.3</td>
</tr>
<tr>
<td>Region 1</td>
<td>n₁</td>
<td>n₁</td>
</tr>
<tr>
<td>Region 2</td>
<td>n₁</td>
<td>n₁</td>
</tr>
<tr>
<td>Region 3</td>
<td>n₁</td>
<td>n₁</td>
</tr>
<tr>
<td>Region 4</td>
<td>n₂</td>
<td>n₁</td>
</tr>
<tr>
<td>Region 5</td>
<td>n₂</td>
<td>n₁</td>
</tr>
<tr>
<td>Region 6</td>
<td>n₁</td>
<td>n₂</td>
</tr>
<tr>
<td>Region 7</td>
<td>n₁</td>
<td>n₁</td>
</tr>
<tr>
<td>Region 8</td>
<td>n₂</td>
<td>n₁</td>
</tr>
</tbody>
</table>

Tuning strategies for modified MMI-switch (structure 6)
Y-junction switch: (DOS)

Imbalance dB = 10\log_{10}\left(\frac{P_1}{P_2}\right)

Splitter efficiency % = \left[\frac{P_1 + P_2}{P_0}\right] \times 100

Advantage:
- Crosstalk improvement using tapered output waveguides
- Use of slanted electrode regions to reduce drive voltage requirement for DOS
Large Switch architectures

Check points:

✓ Crosstalk
✓ Path delay
✓ Coupling power losses
✓ Blocking feature
✓ Rearrangeability
✓ On-chip viability

Crossbar pattern
Non-blocking and rearrangeable modified Banyan network

Interconnected Banyan switch fabric (IBSF):
Non blocking 4×4 MMI–switch with absolute loss uniformity

Average error for respective input power combination (ref. index=3.15)

Mean error value = 4.1 for refractive index 3.15

Mean error value = 1.8508 for refractive index 3.058

Average error for respective input power combination (ref. index=3.058)
Labeled s–bend (concave arc type) section waveguide used with Design-3.

Labeled switch layout with projection of optical beam through desired path (in–port to out–port 1).
Principle of add/drop microring resonator
Designed Gates:

1. AND Gate

2. OR Gate
3. NOR/XNOR Gate
4. XOR Gate
Code Converters

Gray to Binary Code Converter
Progressive research steps:

✓ Reconsideration of the architecture of basic optical elements.

✓ The component architecture to be incorporated with other aspects.

✓ New Designs, simulations with guiding algorithm for higher order architectures with practically viability to the recent demand.

✓ Incorporation of newer devices to enhance applications areas.

✓ Analysis of and improvement in noise resistibility of the particular architectures and the proposed ones.

✓ Photonic crystals /non-linear materials as a building material.
References


Global Initiative of Academic Networks (GIAN)

Aim:

- Tapping the talent pool of scientists and entrepreneurs, internationally to encourage their engagement with the institutes of Higher Education in India so as to augment the country's existing academic resources, accelerate the pace of quality reform, and elevate India's scientific and technological capacity to global excellence.

Funds:

- US$ 8000 for 12/14 hours and US$ 12000 for 20/28 hours (covering travel and honorarium), Local hospitality to be arranged by the Host Institution.